



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,674	10/03/2006	Richard Kabzinski	60136-0011	5546
29989	7590	08/01/2011		
HICKMAN PALERMO TRUONG & BECKER, LLP			EXAMINER	
2055 GATEWAY PLACE				ZIA, SYED
SUITE 550			ART UNIT	PAPER NUMBER
SAN JOSE, CA 95110			2431	
			MAIL DATE	DELIVERY MODE
			08/01/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Attachment to Advisory Action

This office action is in response to amendment and remarks filed on July 1, 2011. The remarks filed have been entered and made of record. Claims 29-32, 34-36, 38-48, and 50-54 are pending.

Response to Arguments

Applicant's arguments filed on July 1, 2011 have been fully considered but they are not persuasive because of the following reasons:

Regarding Claims 29-32, 34-36, 38-48, and 50-54 applicants argued, that system of cited prior art (CPA) [Thibadeau U. S. Patent 7,036,020 and Hearn et al. (WO 03/003242)] does not teach or suggest "*selectively block access to operating system data*", and the references do not "*divert... operating system files to a location different than the security partition*", as recited in Claims.

This is not found persuasive. The system of cited prior art teaches a method for promoting security method in computer system that involves partitioning portion of storage device to form security partition and limiting access to portion of storage device by operating system of computer. In that system, Hearn, discloses a security device comprising a hardware processor or controller for intercepting communications and selectively blocking access to operating system data between the host CPU and the security partition, wherein the security device is deployed along the chain of components that connect the host CPU to the storage device, wherein the security device's processor or controller is distinct from the host CPU [Fig.1 Item 35, Fig.2 and page 15 line 2 to line 8, page 5 line 24 to page 17 line 8].

In this system selective blocking occurs during initialization of the computer and includes intercepting all said data access during the start up sequence immediately after said initialization and before loading of the operating system of the computer to enable independent control of the host CPU and configuration of the computer in a manner so as to prevent unauthorized access to the storage device. The security device CPU 37 operates according to a prescribed application program stored in the flash ROM 41 and which is loaded into the RAM 39 on start up and becomes the operating system for the security device. The CPU 37 communicates with the bus control and interface logic 43, which is interposed in line with the ATA cable 33 to intercept communications between the host CPU 13 and the storage media 21. The secure media interface 45 is interposed between the bus control and interface logic 43 and the custom interface 49 to facilitate communications between the host CPU 13 and the secure storage media 47 under the control of the CPU 37 (Thibadeau :(Fig.1-4, col.4 line 37 to col.6 line 16), and Hearn: Fig.1 Item 35, Fig.2 and page 15 line 2 to line 8, page 5 line 24 to page to page 17 line 8).

As a result, cited prior art does implement and teach a system that relates to securing access in a computer system. Applicants still have failed to explicitly identify specific claim limitations, which would define a patentable distinction over prior arts.

Therefore, the examiner asserts that cited prior art does teach or suggest the subject matter broadly recited in independent Claims and in subsequent dependent Claims. Accordingly, rejections for claims 29-32, 34-36, 38-48, and 50-54 are respectfully maintained.

sz
July 17, 2011
/Syed Zia/
Primary Examiner, Art Unit 2431